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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/851,608	05/05/97	BULUCEA C	M-799-4C-US

MM12/0209

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EXAMINER	
CARROLL, J	
ART UNIT	**PAPER NUMBER**
2811	36

DATE MAILED: 02/09/00

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PAPER NO. 36

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08/851,608
05/05/97

CARROLL
2811

TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING BODY PROFILE AND THREE-DIMENSIONAL GEOMETRY

Before the Board of Patent Appeals and Interferences

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CONSTANTIN BULUCEA *ET AL.*
FOR
APPELLANTS

Examiner's Answer

This is our Answer to the Appeal from the Rejection of Claims under 35 U.S.C. 103 and Double Patenting.

STATUS OF CLAIMS

The Appellants have adequately summarized the status of the Claims on Brief page 2.

STATUS OF AMENDMENTS

The Appellants have adequately summarized the status of amendments on Brief page 2.

SUMMARY OF INVENTION

The Appellants have adequately summarized the disclosed Invention on Brief pages 2 and 3.

ISSUES

The Appellants have adequately summarized Issues 1 through 5 on Brief pages 3 and 4.

The Appellants successfully rendered moot Issue 5 by providing an acceptable Terminal Disclaimer, filed concurrently on 21 June 1999 with an acceptable Appeal Brief.

We hereby allow Claims 22, 23, 38, 42, 59 and 63.

GROUPING OF CLAIMS

The Appellants have adequately grouped the Claims on Brief pages 4 and 5.

CLAIMS ON APPEAL

The Appellants have accurately reproduced the Claims in the APPENDIX on Brief pages 20 through 31.

REFERENCES ON APPEAL

	Patent	Inventor(s)	Publication Date
A.	US 4,420,379	Tonnel	13 December 1983
B.	US 4,376,286	Lidow *et al.*	08 March 1983
C.	US 4,148,047	Hendrickson	03 April 1979
D.	US 4,145,700	Jambotkar	20 March 1979
E.	US 5,072,266	Bullucea *et al.*	10 December 1991

F. K. Lisiak *et al.*, "Optimization of Nonplanar Power MOS transistors," *IEEE Transactions on Electron Devices*, Vol. ED-25, No. 10 (October 1978) pp. 1229-1234.

G. D. Ueda *et al.*, "A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance," *IEEE Transactions on Electron Devices*, Vol. ED-32, No. 1 (January 1985) pp, 2-6.

H. K. Yamabe *et al.*, "Nonplanar Oxidation and Reduction of Oxide Leakage Currents at Silicon Corners by Rounding-off Oxidation," *IEEE Transactions on Electron Devices*, Vol. ED-34, No. 8 (August 1987) pp.1681-1687.

We hereby withdraw application of References B, C, E and F, thereby affecting Issues 1 through 4 as presented in the Appeal Brief on pages 3 and 4.

We maintain application of References A, D, G and H.

NEW PRIOR ART

None

NEW GROUNDS OF REJECTION

None

GROUNDS OF REJECTION AND APPLICATION OF THE REFERENCES TO THE CLAIMS ON APPEAL

Issues 1, 2 & 4

Under 35 U.S.C. 103, Claims 17 through 21, 25 through 29, 32 through 37, 44, 46 through 58, 64 and 65 stand rejected as unpatentable over Tonnel (Reference A) considered with Ueda *et al.* (Reference G).

Tonnel disclosed non-planar MOS transistors that included the V-MOS cell illustrated with Figures 3 through 19 as showing V-shaped slots (30) accordingly accommodating the V-shaped insulated polysilicon gate (grid) electrode (31) (32), and unillustrated U-MOS transistors, evidently from the paragraphs beginning on line 14 of column 1 and on line 61 of column 5. In view of Ueda *et al.* (Figure 1), who taught a vertical power MOS transistor structure that possessed rectangularly-grooved slots accordingly accommodating U-shaped insulated gate electrode, one would have instantly recognized Tonnel's characterization of U-MOS transistors as accordingly possessing U-shaped slots having vertical sides and accommodating U-shaped insulated gate electrode as taught by Ueda *et al.* Thus, we conclude, one would have obviously found that Tunnel anticipated U-MOS cell structures that possessed slots with vertical sides that accordingly accommodated U-shaped insulated gate electrode, but otherwise possessed the same the structure as the V-MOS cell structure illustrated with Figures 3 through 19.

More particularly with reference to Figures 3 through 19, Tonnel with Figure 3 showed a three-dimensional perspective view that included substantial, top-surface topology in the foreground, mid and backgrounds, and V-shaped slots in the foreground as formed deeper than P-type body layer (25) and P-type guard ring layer (22). With remaining Figures 4 through 19, Tonnel showed two-dimensional cross-sectional views at various stages of V-MOS transistor cell manufacture:

a) Figures 4 through 12 showed cross-sections taken in a plane perpendicular to a plane running parallel to the V-shaped slot axis;

b) Figures 17 through 19 showed a particular way of producing the same cross-sections as in Figures 10 and 11;

c) Figures 14 and 16 showed cross-sections taken in a plane coincident with the V-shaped slot axis; and

d) Figures 13 and 15 showed cross-sections taken in a plane running parallel to the V-shaped slot axis but outside the V-shaped slot.

Examining the two-dimensional cross-sectional views, known to be free from geometrical distortions that may arise when depicting in three dimensions as in the perspective view of Figure 3, one finds that Tonnel formed V-shaped slots (30) to be deeper than a PN-junction defining the depth of P-type body region (25) (Figure 12); and one finds that Tonnel formed V-shaped slots to be shallower than a PN-junction defining the depth of P-type guard ring (22) that smoothly joined and became a part of the P-type body region (25).

One would have instantly realized the presence of a geometrical and structural discrepancy between the three-dimensional perspective view of Figure 3, showing V-shaped slots formed more deeply than the P-type body and guard ring regions, and the two-dimensional cross-sectional views showing the V-shaped slots formed more shallow than the P-type guard ring region (22). However, one would have instantly resolved the discrepancy in favor of a deeper guard ring region than a depth of the slots when examining the supporting evidence shown in the cross-sectional view of Figure 16 whereby Tonnel unambiguously disclosed that P-type guard ring region (22) was formed more deeply than the V-shaped slots accommodating the insulated gate electrode (31) (32), interlevel insulating layer (34) and source metallic electrode (33).

Corroborating supporting evidence can be found in the process of manufacturing stages shown in cross-section. Figure 6 showed slots (30) formed at a depth substantially the same as that of guard ring region (22). However, Tonnel required the performance of thermal anneal processes at both the Figure 9 stage to initially diffuse P-type body region (25) and, at the Figure 10 stage, to initially diffuse N-type source regions (26). Notice that P-type body region (25) in the Figure 10 stage diffused further downwardly from its original position shown in the Figure 9 stage due to substantial thermal diffusion to initially form the source regions (26). Of course, P-type guard ring regions (22) also underwent, at the Figure 10 process stage, further downward diffusion deeper than the fixed V-shaped slots (30) because the P-type guard ring regions were also exposed to the same thermal diffusional environment that formed the source regions. Thus, we found consistent corroborating evidence in the disclosed process of manufacture that Tonnel fully anticipated forming P-type guard ring diffusion regions (22) substantially more deeply than the depths reached by the V-shaped slots (30).

Thus, from the preponderance of evidence taken from the Tonnel disclosure as a whole, we conclude that one would have readily achieved not only a V-MOS transistor structure, but also a U-MOS transistor structure whereby the depth of the slots (30) accommodating the insulated gate electrode (31) (32) would have been substantially more deep than the P-type body region portion (25), and would have been substantially less deep than the P-type guard ring region portion (22) that smoothly joined and became a part of more shallow body region (25) initially at the Figure 9 process stage.

With respect to independent Claim 17, Tonnel in view of Ueda *et al.* disclosed a trench (slot) DMOS transistor cell that comprised: N-type substrate (20) (Figure 3); a uniformly doped N-type epitaxial layer (21) possessing a finite thickness formed on the substrate; U-shaped trench slots (30) with substantially vertical sidewalls formed in a top surface of the epitaxial layer; a P-type body region (25) having a depth at a second location less than the trench slot depth; with N-type source regions (26) formed above the body region in the second location horizontally adjacent the trench slots; the P-type body region (25) at a second location smoothly joined with a P-type guard ring body portion (22) near a first location; whereby the P-type guard ring body portion (22) was formed substantially

more deep than the trench slot depth; whereby a lateral distance between the trench slot (30) and the P-type body region portion (25) at a second location was substantially less than a distance between the trench slot (30) and the guard ring body portion at a first location (22). Observing that the structural combination required by Claim 17 would have been readily achieved by one simply following the expressed teachings and suggestions of Tunnel and Ueda *et al.*, as fully discussed *supra*, we conclude that one also would have readily achieved the claimed property that transistor breakdown occurred across the epitaxial layer closer to the first location than to the second location, because the claimed property itself would have constituted a property inherent in the prior art trench (slot) DMOS transistor. The present situation, therefore, comes under the Court's directive that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art, after at least *In re Swinehart*, 169 USPQ 226 (CCPA 1971); *In re Best*, 195 USPQ 430 (CCPA 1977).

In re dependent Claims 20, 21 and 26, observing that the structural combinations required would have been readily achieved by one simply following the expressed teachings and suggestions of Tunnel considered with Ueda *et al.*, as discussed *supra*, we conclude that one also would have achieved the claimed property that transistor breakdown occurred closer to the first location than to the second location.

In re dependent Claims 27 and 28, Tonnel evidently opened up a formerly, closed cell configuration by cutting away unillustrated sections as in the three-dimensional perspective view of Figure 3.

With respect to independent Claim 32, Tonnel in view of Ueda *et al.* disclosed a trench DMOS transistor cell that comprised an epitaxial layer (21) located above substrate (20) whereby trench slots (30) having substantially vertical sidewalls were formed in the epitaxial layer to a predetermined depth, whereby body regions (25) smoothly joined guard ring regions (22) that possessed a maximum depth greater the predetermined depth of the trench slots. Observing that the structural combination required by Claim 32 would have been readily achieved by one simply following the expressed teachings and suggestions of Tonnel considered with Ueda *et al.*, we conclude that one also would have readily achieved

the claimed property that transistor junction breakdown occurred away from the trench slots and into the epitaxial layer, because the property itself would have inherently constituted the prior art trench DMOS transistor cell construct. Thus, the present situation comes under the Court's directive that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art.

With respect to independent Claim 46, Tonnel in view of Ueda *et al.* disclosed a transistor that comprised: an N-type first region (20) (21); a P-type second region (25) (22) formed over the first region; an N-type third region (26) such that the first (20) (21) and third (26) regions were separated from one another by the second region (25) (22); a U-shaped trench slot (30) having substantially vertical sidewalls and extending through the third (26) and second (25) (22) regions; an insulated gate (32) (31) located in the trench slot; whereby P-type portion (22) of the second region was spaced from the trench slot (30) and extended deeper than the trench slot (30). If one had expected to use the transistor, which would have expected of one possessing ordinary skill in the transistor art, one would have applied a predetermined voltage to the gate and third region and another predetermined voltage to the first region. If avalanche breakdown occurred, we conclude that it would have occurred away from a trench surface because such a property would have inherently flowed from the transistor structure claimed inasmuch as the transistor structure claimed would have been readily achieved by one simply following the expressed teachings and suggestions of Tonnel and Ueda *et al.* Thus, the present situation comes under the Court's directive that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art.

In re dependent Claim 49, the inherent avalanche breakdown property claimed would have inherently corresponded to the claimed reach-through breakdown across the second portion because Tonnel anticipated forming a first region that comprised an N-type second portion (21) having a lesser dopant concentration than that of N-plus-type first portion (20).

In re dependent Claim 50, Tonnel qualitatively showed that the depth of trench slot (30) was substantially exceeded by the depth of P-type second region

portion (22); Ueda *et al.* quantitatively taught (last paragraph of the left column on page 5) that the U-shaped slot depth of about 3.5 microns exceed the depth of planar P-type second region by about 0.5 micron. Since the cross-sectional view of Tonnel showed P-type second region portion (22) exceeded the depth of slot (30) by approximately as much as the depth of slot (30) exceeded the depth of P-type second region (25), we conclude it to have been obvious for one to have accordingly disposed the depths of P-type second region portion (22) and trench slot (30).

With respect to independent Claim 52, Tonnel in view of Ueda *et al.* disclosed a transistor that comprised: an N-plus-type first region (20); an N-type second region (21), having a lesser dopant concentration than the first region, formed over the first region; a P-type third region (25) (22), having a deepest part (22), formed over the second region so that a PN-junction resided between the second and third regions, the PN-junction having a planar portion associated with at least third region portion (25); an N-type fourth region (26) formed over the third region (25); a trench slot (30), accommodating an insulated gate electrode (32)(31), having substantially vertical sidewalls, and extending through the fourth (26) and third (25) regions; whereby the deepest part of the third region (22) was laterally spaced from the trench slot (30); whereby a finite distance obtained between the deepest part of the third region (22) and first region (20). In use, the transistor disclosed by Tonnel in view of Ueda *et al.* would have possessed a depletion layer width associated with the PN-junction under reverse bias, and would have been capable of breaking down at sufficient applied voltage. The claimed property that the distance would have been less than the depletion width at breakdown, itself would have constituted an inherent property of the prior art transistor because one would have readily achieved the structural subject matter claimed by simply following the expressed teachings and suggestions of Tonnel in view of Ueda *et al.* The present situation, therefore, comes under the Court's directive that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art.

With respect to independent Claim 54, Tonnel in view of Ueda *et al.* disclosed a semiconductor device that comprised: a semiconductor substrate N-type drain region (20) (21); a P-type body region (25) (22) formed in the N-type substrate to locate a PN-junction therebetween at a maximum depth at body region

(22); a source region (26); a trench slot (30), having substantially vertical sidewalls, formed in the substrate to a particular depth less than the maximum depth of body region (22); the trench slot (30) accommodating a gate region (32) separated from the body region by gate dielectric material (31) located between the gate (32) and body (25) (22) regions. The claimed property that a PN-junction breakdown would have occurred away from the trench, itself would have constituted an inherent property of the prior art semiconductor device because one would have readily achieved the structural subject matter claimed by simply following the expressed teachings and suggestions of Tonnel in view of Ueda *et al.* The present situation, therefore, comes under the Court's ambit that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art.

In re dependent Claim 65, Tonnel disclosed a body region (25) (22), in the horizontal, cross-sectional view of Figure 12, that possessed a polygonal shape.

Under 35 U.S.C. 103, independent Claim 30 stands rejected over Tonnel (Reference A) in view of Ueda *et al.* (Reference G), as discussed *supra*, but further considered with Jambotkar (Reference D). More particularly, Tonnel in view of Ueda *et al.* disclosed a trench (slot) DMOS transistor cell that comprised: an N-plus-type substrate (20) having a top surface; an N-type first covering layer (21) contiguous with the substrate and overlying its top surface; whereby the dopant concentration (N) of the first covering layer (21) is less than the dopant concentration (N+) of the substrate (20); a P-type second covering layer (25) (22) extending vertically downward from its top surface, contiguous with a top surface of the N-type first covering layer (21), and extending into an upper portion of the N-type first covering layer (21); whereby a PN-junction was established between the N-type first covering layer (21) and the P-type second covering layer (25) (22); an N-type third covering layer (26) with its top surface contiguous with and partly overlying the top surface of the P-type second covering layer (25); whereby P-type second covering layer (22) has a maximum depth relative to the top surface of the N-type third covering layer (26); a U-shaped trench slot (30), having side and bottom walls, extending vertically downward from the top surface of the N-type third covering layer (26), through the N-type third (26) and P-type second (25) covering layers, and through a portion, but not all the way through the N-type first

covering layer (21); whereby the trench slot (30) depth relative to the top surface of N-type third covering layer (26) was substantially less than the maximum depth of P-type second conductive layer (22); a layer of oxide (31) positioned within trench slot (30) and contiguous with the side and bottom walls thereof so that the trench was filled with the oxide layer; electrically conductive polysilicon semiconductor material (32) positioned within trench slot (30) contiguous with oxide layer (31) so that oxide layer (31) stood between the conductive polysilicon gate grid electrode (32) and the side and bottom walls of trench slot (30); and, as shown in Figure 3, polysilicon electrode (24) electrically coupled to polysilicon gate grid electrode (32), and a metal electrode (33) electrically coupled to N-type third covering layer (26). Tonnel showed no electrode electrically coupled to N-plus-type substrate (20). However, Jambotkar, who taught a non-trench vertical DMOS transistor cell that possessed an N-plus-type substrate (10), electrically coupled thereto another electrode (44). Thus, we conclude, it to have been usual practice for one to have electrically coupled an electrode to an N-plus-type substrate of a vertical DMOS transistor cell. Therefore, it would have been usual practice for one to have accordingly electrically coupled another electrode to N-plus-type substrate (20) of Tunnel. If one were to have used the trench slot DMOS transistor cell as disclosed by Tonnel, Jambotkar and Ueda *et al.*, then one may have applied sufficient voltage to have caused electrical breakdown at the PN-junction established between the P-type second (25) (22) and N-type first (21) covering layers. Under electrical breakdown condition, the breakdown would have occurred at a portion (22) of the P-type second covering layer away from the trench slot (30). Such a property, we conclude, must have occurred in the prior art trench DMOS transistor cell construct because the whole of the presently claimed trench DMOS transistor cell construct would have been obtained by one simply following the expressed teachings and suggestions of Tonnel in view of Ueda *et al.* and considered further in view of Jambotkar. The present situation, therefore, falls within the Court's ambit that a newly discovered property inherently possessed by things in the prior art does not cause a Claim drawn to those things to distinguish over the prior art.

Issues 3 & 4

Under 35 U.S.C. 103, Claims 31, 39, 40, 41, 60, 61 and 62 stand rejected over Tunnel (Reference A), Ueda *et al.* (Reference G) and Jambotkar (Reference D) as applied *supra* against independent Claims 30, 32 and 54, but further considered with Yamabe *et al.* (Reference H). With respect to Claims 31, 39 and 60, Yamabe *et al.* found, in MOS transistors that comprised insulated gate electrodes accommodated within U-shaped trench slots such as those anticipated by Tonnel, the advantage of reduced gate oxide leakage current at silicon corners previously rounded by the removal of a sacrificial thermal oxide. One therefore would have recognized it to have been desirable to have achieved the same advantage when using the trench DMOS transistor constructs disclosed by Tonnel in view of Ueda *et al.*, and Tonnel in view of Ueda *et al.* and Jambotkar. Thus, we conclude, it to have been obvious for one to have accordingly achieved the desirable advantage found by Yamabe *et al.* by accordingly rounding the trench, U-shaped slots (30) before applying the insulated gate electrode (31) (32) therein.

In re Claims 40, 41, 61 and 62, after Yamabe *et al.*, one would have rounded U-shaped trench slots (30) at their corners by applying and removing a sacrificial thermal oxide prior to application of gate oxide layer (31) and conductive polysilicon gate electrode (32). Thus, one would have readily achieved the subject matter claimed by simply following the expressed teachings of Yamabe *et al.* combined with the semiconductor device disclosed by Tonnel in view of Ueda *et al.*

RESPONSE TO ARGUMENTS MADE IN THE APPELLANTS' BRIEF ON APPEAL

The Appellants' essential argument centered upon the Tonnel disclosure, especially the transistor cell structure as disclosed in Figures 3 through 19. Interestingly on Brief page 6, while acknowledging **the fact** that Figure 12 showed a completed cell in cross-section that included P-type region (22) deeper than slot (30), the Appellants at once faulted Tonnel's written disclosure for not explicitly calling attention to the fact in a manner that would satisfy some unmentioned but, no

doubt, rather arbitrary standard of disclosure held by the Appellants. Incongruously, the Appellants then concluded that we somehow invoked hindsight speculation when interpreting **the fact** embodied in Figure 12. Consistently, however, the Appellants in the foregoing record steadfastly held to the theory that the three-dimensional, perspective view most accurately represented the Tonnel transistor, rather than the structures disclosed with the cross-sectional views of Figures 4 through 19.

In response, we fail to understand the logical principle the Appellants evidently perceived as underpinning their interpretation of Tonnel. Considering the fact that Tonnel neither expressed in words that P-type region (22) was less deep than slot (30), we would be interested in the Appellants' explanation as to why they, at once, have not invoked a hindsight speculative theory regarding the transistor cell structure that conveniently fell outside the metes and bounds of their claimed subject matter at issue, while we, instead, have in some yet-to-be-explained manner used hindsight speculation.

Of course, we have scrupulously stayed away from the forbidden aspects of hindsight. Instead, we identified a discrepancy regarding the apparent relative depths of slot (30) and P-type region (22) between that as illustrated in three-dimensional perspective view of Figure 3, and the apparent depths illustrated in the cross-sectional views of the remaining drawings; and we resolved the discrepancy based upon an objective analysis of the Tonnel disclosure taken as a whole. Any objective interpretation of the completed device of Figure 12 would have included a depth relationship within the scope of the Claims at issue. Any objective interpretation of the completed device of Figure 16 would have included as fact that P-type region (22) was deeper than slot (30), while P-type region (25) was less deep than slot (30) and, thus, not in view. Therefore, there are two pieces of evidence provided in the Tonnel disclosure that unambiguously suggested that one should form P-type region (22) deeper than slot (30). Thus, the two pieces of evidence effectively counterposed the suggestion embodied in the three-dimensional perspective view of Figure 3 that P-type region (22) was more shallow than slot (30). Further, Tonnel provided a corroborating third piece of evidence that effectively counterposed the relative depths of slot (20) and P-type region (22) as illustrated in the three-dimensional perspective view of Figure 3, when Tonnel

explained the method of manufacturing the transistor cell that included, after diffusing P-type region (22) (Figure 5), the performance of two annealing steps to promote diffusion P-type region (25) (Figure 9), and to promote the diffusion of N-type source region (26) (Figure 10). Importantly, the two subsequently performed diffusions of Figures 9 & 10 also would have further diffused to a level deeper than fixed slot (30), deepest P-type diffusion (22), as consistently shown in each of Figures 10, 11 and 12. Where's the forbidden hindsight in the objective analysis *supra*? NOWHERE.

CONCLUSIONS

Thus, from the preponderance of evidence taken from an objective analysis of the Tonnel disclosure as a whole, we have concluded that the three-dimensional, perspective view of Figure 3 erroneously suggested that one should form P-type region (22) less deep than slot (30). We have further concluded thereby that the Tonnel unambiguously disclosed not only the semiconductor transistor devices, but also a means to achieve the semiconductor transistor devices claimed wherein P-type region (22) was more deep than slot (30) accommodating the insulated gate electrode. We have still further concluded, as evidenced by the Brief, that the Appellants have failed to come to grips with the fact that the applied prior art as a whole rendered obvious, within the meaning of 35 U.S.C. 103, the claimed subject matter remaining at issue.

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We therefore respectfully request the esteemed members of the USPTO Board of Patent Appeals and Interferences to affirm the Final Rejection.

Respectfully submitted.

James J. Carroll
Primary Examiner